InAs nanowire with epitaxial aluminium as a single-electron transistor with fixed tunnel barriers

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Abstract

We report on fabrication of a single-electron transistor using InAs nanowires with epitaxial aluminium with fixed tunnel barriers made of aluminium oxide. The device exhibits a hard superconducting gap induced by the proximized aluminium cover shell and it behaves as its metallic counterpart. We confirm that unwanted extra quantum dots can appear at the surface of the nanowire, but can be prevented either by covering the nanowire with aluminium, or by inserting a layer of GaAs between the InAs and Al. Our work provides another approach to study proximized semiconducting wires.

Semiconducting nanowires (NWs) are widely used nowadays in nanotechnology [1–3] as their transport properties can be easily tuned [4, 5]. In particular, InAs NWs are of interest as they are optically active [6] and can act as a field-effect transistor [7], a quantum dot [8–13] or a qubit [14]. When superconductivity is induced by proximity effect, this system appears to be a promising candidate in the search of Majorana bound states [15–17]. Recently, the growth of a NW with a high quality interface between InAs and aluminium has been successfully achieved [18], with a hard superconducting gap [19]. However, despite the high quality of the NW, the presence of unwanted quantum dots (QDs) has been reported [19–21] and is believed to be caused by defects [22] and potential fluctuations at the surface of the NW [23]. In devices with electrostatic barriers, the contacts are made directly on InAs and the Al cover is etched away for this purpose, leaving only an Al "island" (see, e.g., the device in Ref. [24]). In order to have an ohmic contact, additional chemical or plasma cleaning of the surface may be needed. These processes may deteriorate the surface of InAs, increasing thus the likelihood of forming of an unwanted QD. It is nevertheless possible to make this QD transparent by tuning locally its potential with additional side gates. However, the location and size of the unintentional QD are not controlled. The devices may be artificially complex by adding side gates, which are potentially unnecessary. A solution to prevent the QD formation is to cover the InAs NW with a protective shell, with the condition that this shell should not affect other properties of the device. Although it is possible to form ohmic contacts directly on InAs, this extra protective shell should also be compatible with good contacts to the external leads made afterwards.

In this Letter, we present a simple device in an InAs NW proximized with epitaxial Al. Our design prevents the presence of an unwanted QD, while needing only one gate per intentional QD and ensuring good contacts between the NW and the external leads. The main idea is to use the aluminium shell on top of the InAs NW to form a fixed tunnel barrier, thus with InAs as a single electron transistor (SET), as in a metallic system [25, 26]. One advantage of the SET is its simple concept: fabrication generally requires only few steps with reproducible samples and only one gate near the island is needed to tune its potential. Several works already exist on the fabrication of a SET using semiconducting NWs with fixed tunnel barriers (i.e. not tunable by gate modulation), with, e.g., Si NWs [27, 28] or InAs/InP heterostructures [29]. The advantage of our method is that the InAs as well as the interface between InAs and Al remain intact. The fact that the Al is used to form

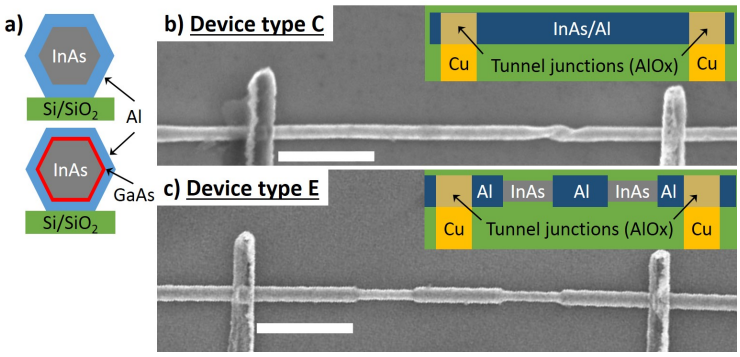

FIG. 1. Panel **a)**: Sketch of the cross-section of the NW. The aluminium shell is grown epitaxially either directly on the InAs wire (upper sketch, devices named "-Al"), or on an intermediate protective GaAs shell (lower one, named "-GaAs"). Panels **b)** and **c)**: Sketch and SEM image of a device type C, with a fully covered wire, and of a device type E, with an isolated aluminium island. The leads and the side gate (not shown) are made of copper, with a thickness from 150 to 200 nm and the tunnel barriers formed of aluminium oxide. The white bars represent 1 μm.

the barriers has two benefits: the Al shell does not have to be etched chemically and the contacts are made directly on it, even with the presence of an intermediate protective layer. The former prevents the formation of additional unwanted QDs and the latter guarantees the possibility to get good contacts. The combination of a metallic SET and a proximized InAs NW can give access to new functionalities.

The hexagonal InAs NWs are grown by molecular beam epitaxy using gold nanoparticles catalyst and are $5-10\,\mu$m long. The aluminium is then deposited epitaxially, covering entirely the NW, without breaking the vacuum to guarantee a good interface between InAs and Al [18]. For some NWs, a buffer layer of GaAs, 5 nm thick, is grown on top of the InAs, followed then by the Al deposition. These NWs form a stacking-fault free wurtzite phase, with misfit dislocations at the InAs/GaAs interface due to the 7% lattice mismatch, therefore the strain relaxes very quickly [30]. This intermediate GaAs layer is expected to reduce the stress at the surface of the InAs and improve the intrinsic properties of the NW (like e.g. carrier mobility), as already observed in various NWs with cover shells [31–35]. A sketch of the cross section of the wires is shown Fig. 1**a)**. The devices with the GaAs covered shell are named "-GaAs", and the others, with only the aluminium shell, are named "-Al". We remind that the NWs with the GaAs layer also have an epitaxial layer of Al.

The NWs are transferred from the growth chip on a pre-marked substrate by dry deposition. The substrate is a highly-doped silicon wafer covered by 200 nm of silicon oxide and is used as a backgate. The position of the NWs is found on the chip using a scanning electron microscope (SEM). In order to study the effect of the chemical etching, we first isolate an Al island ($\sim 1\,\mu$m long) in the middle of the NW, by etching chemically at two places a 0.5 to 1 μm segment of the Al shell by immersion in MF-CD-26 for 90 s at room temperature (called device "E", for Etched). The remaining Al on the central island and on each side of the wire, close to the junctions, is supposed to keep the proximized superconductivity intact and uniform over the entire NW. The other type of devices is made without the chemical etching, keeping the aluminium shell intact and thus without any bare InAs (called device "C", for Covered). The two leads and the side gate are patterned by electron-beam lithography and deposited by electron-beam evaporation. The native oxide layer on Al is removed by argon plasma etching inside the evaporator chamber. The Al is then re-oxidised under O_2 atmosphere of 2 mbar for 2 minutes to create the tunnel junctions. 150 to 200 nm of Cu is next evaporated in order to make the leads and the side gate. The fact that the native Al oxide is etched *in-situ* ensures good control of the tunnel junctions. The junctions cover approximately 100 nm over the wire and are spaced by 5 μm. The sketches and SEM images of the devices are shown Figs. 1**b)** and **c)**. The main properties of the samples are given in Table I. The NWs from the devices E-Al and C-Al come from the same growth, and the same applies for the devices E-GaAs and C-GaAs. Note that only the backgate was used in this study, but we have obtained similar results using the side gate.

We first study the device E-Al, Fig. 1**b)**, in which the InAs core is exposed. Here, we choose the wire without GaAs, and etch Al in selected areas. The effect of the backgate on electron transport measurements is shown in Fig. 2. At negative backgate values $V_{BG} < 0$ (not shown), the transport is blocked. For $0 < V_{BG} < 2$ V, a complex stability diagram is present, with at least two sets of Coulomb diamonds (see e.g. the white dotted and dashed diamonds in the left-hand side of Fig. 2). Only one QD is expected with a small charging energy due to the rather low resistance of the device and the large size of the QD and of the junctions. However, the QDs measured at intermediate gate values, around 1.2 V, show a charging energy between 0.3 and 0.8 meV, too high to reflect the main dot. These large values as well as the aperiodicity of the diamonds with V_{BG} are signatures of

Name	R_T (MΩ)	Δ (μeV)	E_c (μeV)	ϕ_{InAs} (nm)	t_{Al} (nm)	t_{GaAs} (nm)
E-Al	0.16	$< 150^a$	40^a	70	20	n/a
C-Al	0.070	180	20			
E-GaAs	0.065	185	< 10	50	25	5
C-GaAs	20	185	120			

[a] Taken at $V_{BG} = 2\,\mathrm{V}$

TABLE I. Summary of the main properties of devices: the resistance across the whole device at room temperature R_T, the superconducting gap Δ, the charging energy E_c, the diameter of the InAs core ϕ_{InAs}, the thickness of the aluminium layer t_{Al} and of the GaAs layer t_{GaAs}.

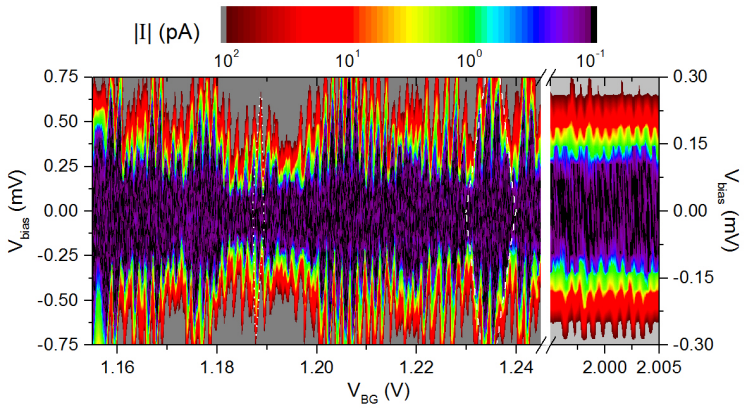

FIG. 2. Current I vs bias V_{bias} and backgate V_{BG} for V_{BG} centred at 1.2 and 2 V, respectively. Several sets of Coulomb diamonds are visible, with different gate periodicity and amplitude, see e.g., the white dashed and white dotted diamonds. Note the different vertical scales between the left and the right part of the graphs.

the presence of several QDs. Above $V_{BG} \sim 2\,\mathrm{V}$, although deformed, the stability diagram is more regular and periodic with V_{BG} (right-hand side of Fig. 2), similar to a metallic device. This corresponds to the intended dot with a charging energy of $\sim 40\,\mu$eV when the unwanted ones are transparent due to the large value of the backgate voltage. The superconducting gap is, however, small in this device compared to the other ones (see Tab. I). One possible reason for this is that the extra QDs affect the superconducting state of the NW. Similar behaviour has been observed in several devices of the same type.

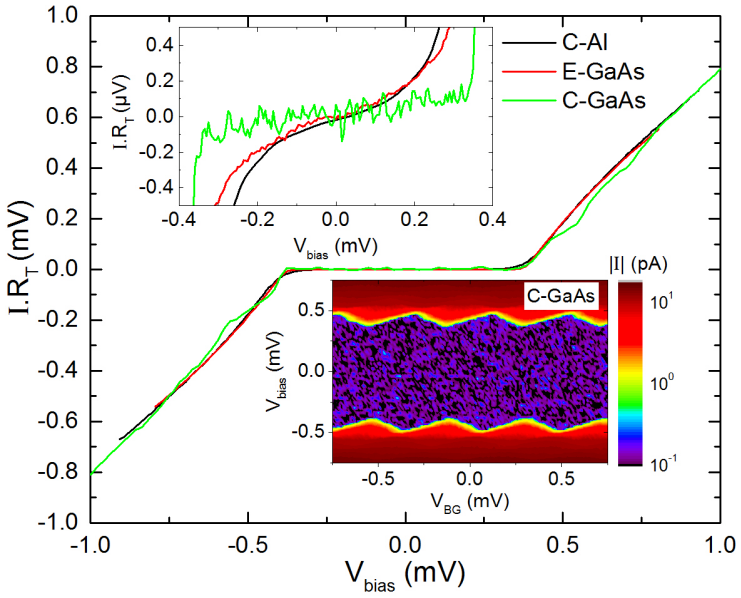

FIG. 3. I-V characteristics of the device C-Al, E-GaAs and C-GaAs. The vertical axis is the product of the current and the resistance of the device $I \cdot R_T$ to scale the measurements. The upper inset is a magnification in the subgap state, and the lower one the stability diagram of the device C-GaAs.

In other devices, the InAs core is unexposed and always covered by another layer, either by the Al shell (device C-Al), by a protective GaAs shell (device E-GaAs) or by both (device C-GaAs). In the linear ohmic regime, at large bias voltage values (not shown), these devices exhibit a metallic behaviour: the transport is independent of the backgate value (no noticeable differences have been seen for V_{BG} in the range -5 to $5\,\mathrm{V}$).

Transport measurements at low bias voltage for the three devices are shown Fig. 3. To scale the measurements, we plot the product of the current and the resistance $I \cdot R_T$. The three devices are similar with the main difference being the charging energy. In the lower inset the stability diagram of the device C-GaAs is shown, exhibiting periodic and regular Coulomb diamonds comparable to what can be obtained in a metallic device. The charging energies of the two other devices are too small to distinguish a clear gate dependence in their transport properties. The upper inset shows the magnification of the measurements in the superconducting state. All devices have a superconducting gap compared to that of Al, $\sim 180\,\mu\mathrm{eV}$, and display a finite slope in the superconducting state, which is a signature of the hardness of the gap. The ratio between the conductance in the superconducting state

G_S and in the normal state G_N is $G_S/G_N \lesssim 10^{-3}$, a measure of the hard gap of our system. The hard gap is not affected by etching the Al shell in the device E-GaAs, since the value measured equals to the gap at the proximity of the junctions, where the Al shell is not etched chemically.

The devices we show can be used for future studies of the properties of proximized superconductivity as our method is relatively non-invasive. Until now the SET regime in proximized InAs NWs was only achieved by tuning the potential of the wire with gates [24], and here the transport properties of the system can be very sensitive to the gate positions, and corrections have to be applied in case of cross-talk between the leads and the gates or between each gate. With one gate only, this is not the case, and we thus have a possibility to perform more advanced experiments, such as using the devices as a turnstile [36]. In two of the devices presented here, the charging energy was too small to perform accurate gate dependence measurements, but it can be easily increased by decreasing the dimensions of the NW (total length and diameter), the size of the QD (junctions spacing) or the size of the junctions.

The similarity between the devices C-Al and C-GaAs provides evidence that NWs with GaAs cover shell can be used for an SET setup, and the similarity between the devices C-GaAs and E-GaAs demonstrates that the GaAs layer prevents the formation of extra QDs. This will give the opportunity to focus in the future on the intrinsic properties of the wires using devices with electrostatic barriers or with half-covered NWs with Al. In these cases, Al etching is necessary, the GaAs cover shell may be used to prevent the appearance of unwanted QDs without affecting the proximity effect. From the present results, it cannot yet be concluded if the GaAs cover shell improves the intrinsic properties of a NW (higher mobility of carriers or "harder" superconducting gap).

In conclusion we have demonstrated that InAs nanowires proximized with aluminium can be used as a single-electron transistor with a hard superconducting gap, by forming a fixed tunnel barrier based on the aluminium shell. Our results confirm that unwanted quantum dots can appear on the surface of the InAs core when bare. As for our devices, the aluminium shell does not have to be etched, and this prevents the formation of these extra quantum dots. This provides an opportunity to use an InAs NW as an island of a single-electron

transistor with the rich properties of a NW. The extra quantum dots can be avoided when an additional thin protective layer of GaAs is inserted between the InAs and the aluminium, without seemingly degrading the transport or the superconducting properties of the system. Our technique provides a way to minimize the number of gates needed to nanowire-based devices.

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